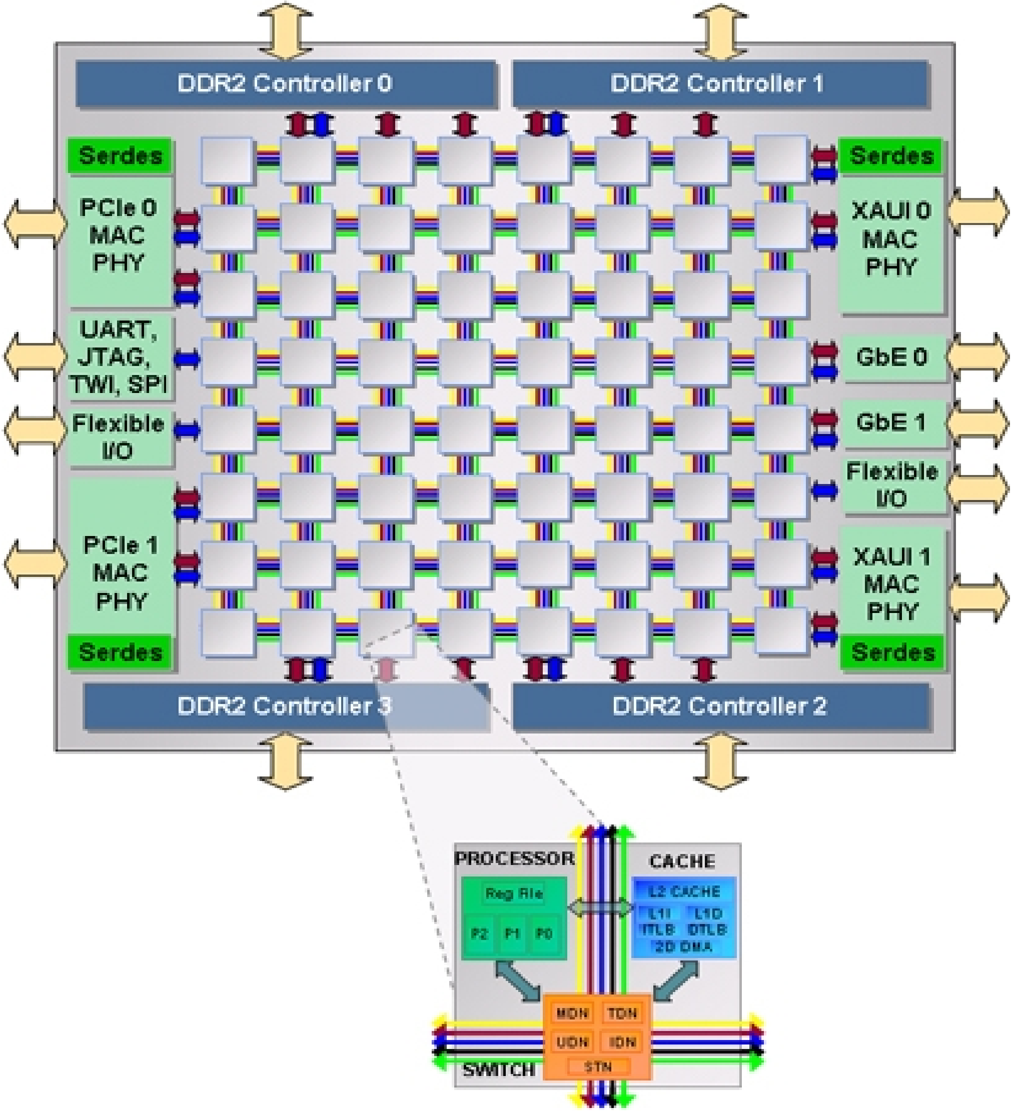
Agenda

- **Part 1**
  - Introduction to MDD for RT/E systems & MARTE in a nutshell
- **Part 2**
  - Non-functional properties modeling
  - Outline of the Value Specification Language (VSL)
- **Part 3**
  - The timing model
- **Part 4**
  - A component model for RT/E
- **Part 5**
  - Platform modeling
- **Part 6**
  - **Repetitive structure modeling**
- **Part 7**
  - Model-based analysis for RT/E
- **Part 8**
  - MARTE and AADL
- **Part 9**
  - Conclusions

Embedded System Hardware is now *Repetitive*



- **Multicore**
  - Today 4 to 8 cores
  - Tomorrow: 16 to 64 cores
- **Processor meshes**
  - Ex: Tilera Tile64
- **SIMD units**
  - Data parallelism

The Future of Embedded Applications is *Parallel*

- **Multimedia**
  - Video coding/decoding
  - HDTV
- **Detection systems**
  - Radar
  - Sonar
- **Telecom**
  - Software radio
  - Wireless communications

Computation models

- Multidimensional signal processing
- Stream processing
- Data parallelism

Repetitive Structure Modeling

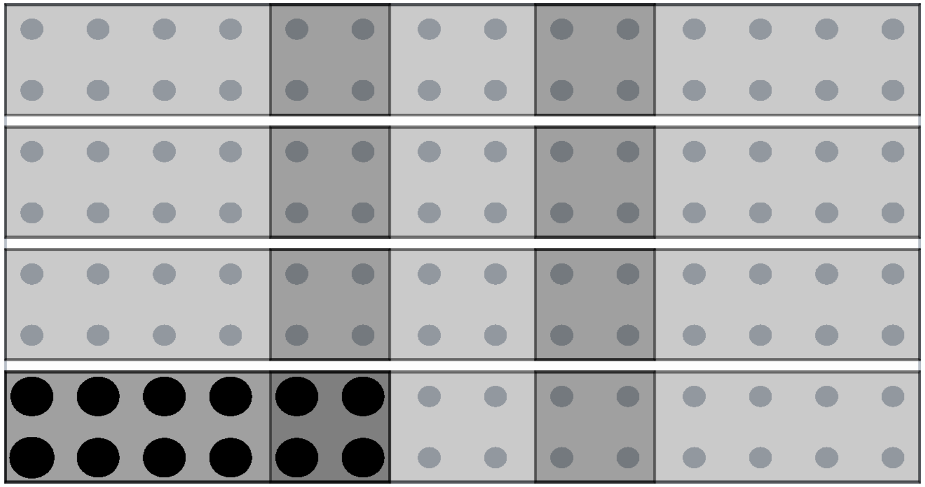
- ## Motivation
  - ***Multidimensional regular parallelism***
    - Nested loops
    - Multiprocessor Systems
  - ***Compact representation***
    - Application
    - Hardware platform
    - Association

- ## Form
  - New notation / stereotypes

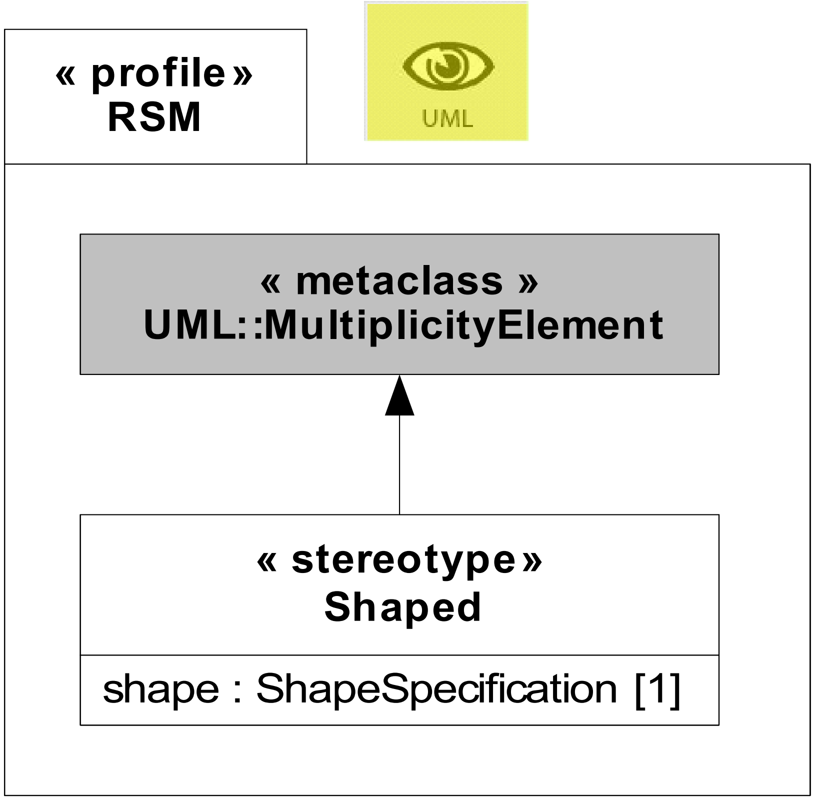
Concepts of Repetitive Structure Modeling

- Concepts
  - **Shape** (extension of *multiplicity*)
    - To model multidimensional arrays
  - **Link topology** (extension of *connector* and *allocate*)
    - To model the topology of the links between multidimensional arrays
    - Pattern-based regular topologies

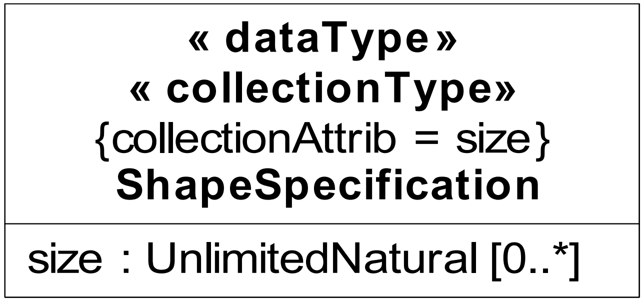
- **Basic idea: *regular tiling* of multidimensional arrays by multidimensional sub-arrays**
  - Regular spacing of points inside a tile
  - Regular spacing of tiles
  - Inherits from the Array-OL language



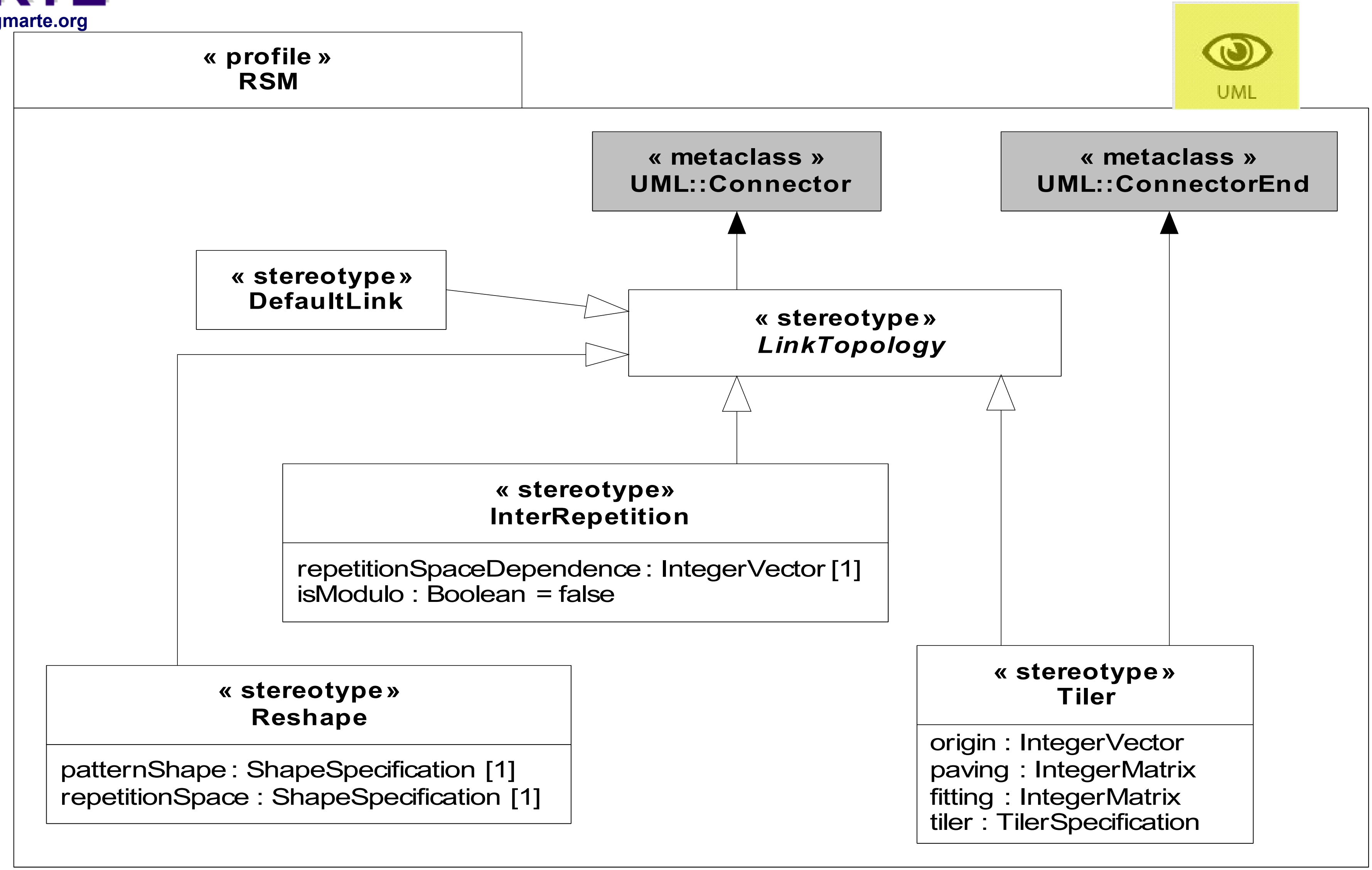
Shape Modeling



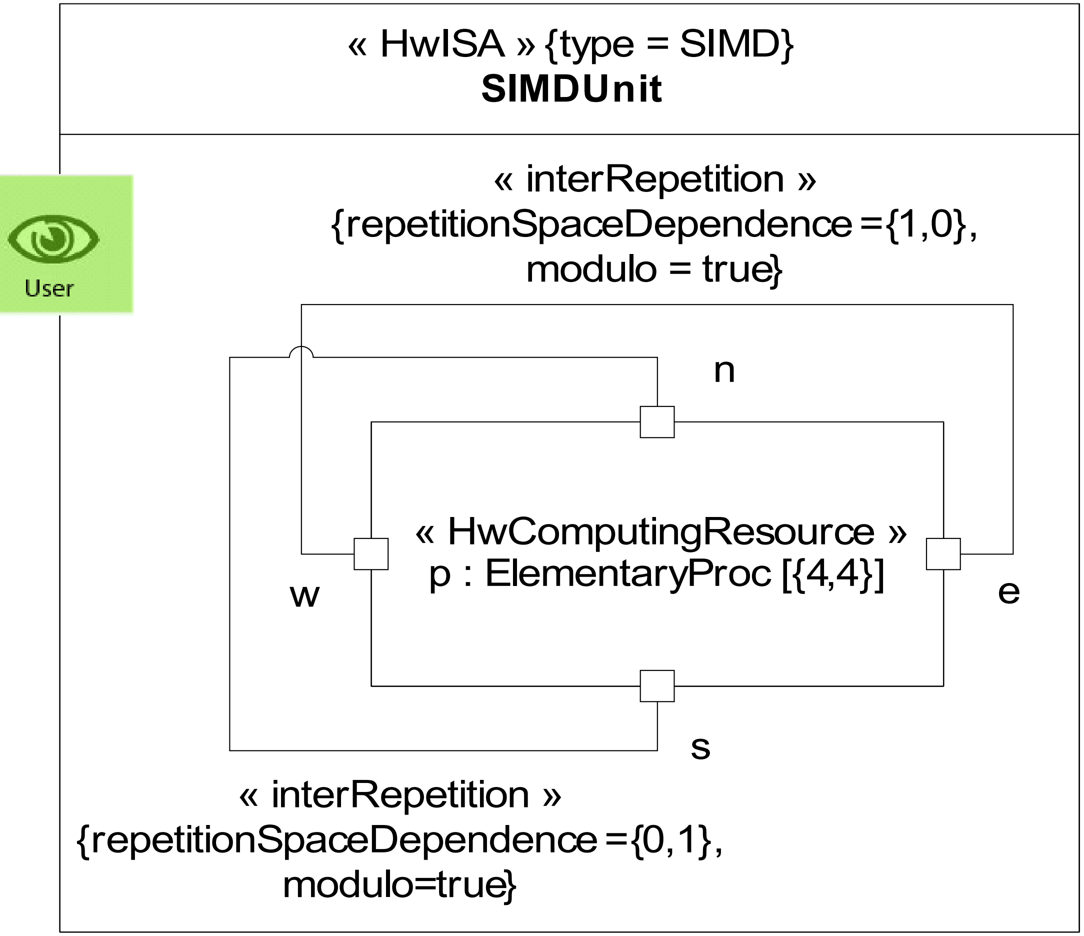
- **New notation**
  - Refinement of the multiplicity notation
  - Vector of UnlimitedNaturals
- **Examples**
  User
  - 16 → {4,4}
  - * → {512,128,*}



Link Topology Modeling

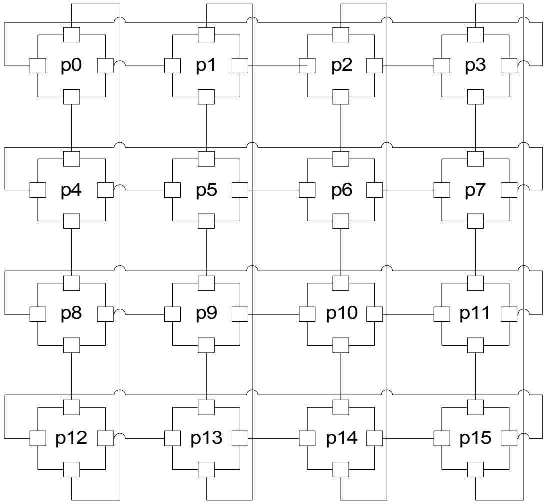


Hardware Platform Example

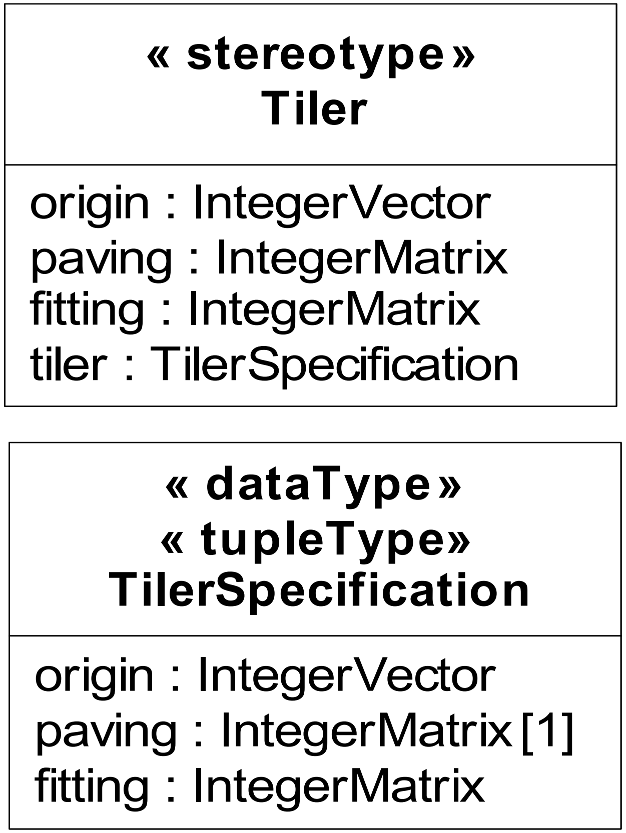


User

- **SIMD unit**
  - 16 processors
- **Topology**
  - Toroidal 4×4 grid
  - Bidirectional connections
    - North-South
    - East-West



Tiling an Array



« stereotype »
Tiler

origin : IntegerVector
paving : IntegerMatrix
fitting : IntegerMatrix
tiler : TilerSpecification

« dataType »
« tupleType»
TilerSpecification

origin : IntegerVector
paving : IntegerMatrix [1]
fitting : IntegerMatrix

- **Needed shapes**
  - Array shape
  - Pattern shape
  - Repetition space shape
- **Tiler**
  - *Fitting*: regular spacing of the points of the tiles
    - Index ***i***
    - Scanning the pattern
  - *Paving*: regular spacing of the tiles
    - Index ***r***
    - Scanning the repetition space

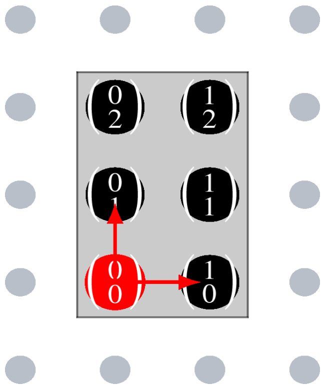
$$\text{origin}+(\text{paving fitting}).\begin{pmatrix} r \\ i \end{pmatrix} \mathit{mod}\ \text{array.shape}$$

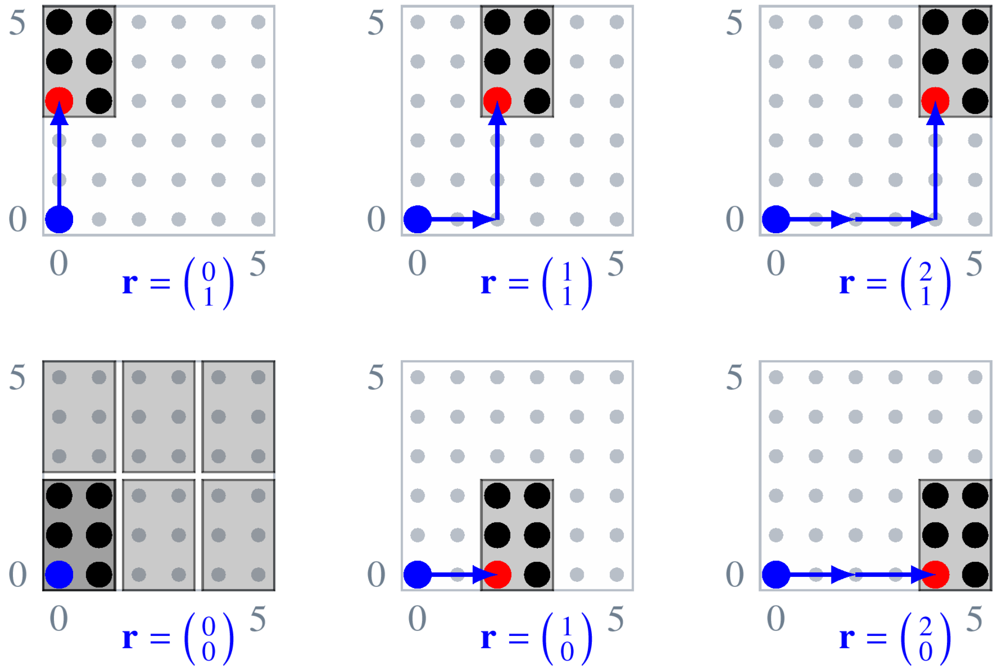
Graphical Interpretation of a Tiler (1/2)

$$F = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \qquad \mathbf{s}_{\text{pattern}} = \begin{pmatrix} 2 \\ 3 \end{pmatrix}$$

$$\mathbf{o} = \begin{pmatrix} 0 \\ 0 \end{pmatrix} \qquad \mathbf{s}_{\text{array}} = \begin{pmatrix} 6 \\ 6 \end{pmatrix}$$

$$P = \begin{pmatrix} 2 & 0 \\ 0 & 3 \end{pmatrix} \qquad \mathbf{s}_{\text{repetition}} = \begin{pmatrix} 3 \\ 2 \end{pmatrix}$$





$\mathbf{r} = \binom{0}{1}$ $\mathbf{r} = \binom{1}{1}$ $\mathbf{r} = \binom{2}{1}$

$\mathbf{r} = \binom{0}{0}$ $\mathbf{r} = \binom{1}{0}$ $\mathbf{r} = \binom{2}{0}$

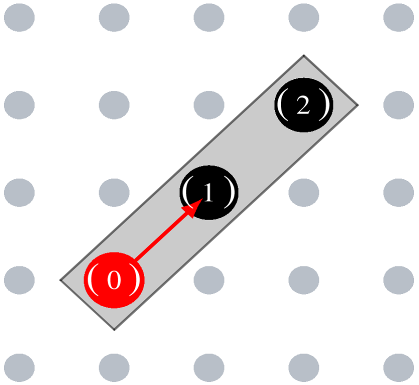
- **Fitting**
  - Column vectors
    - Basis of the tile
  - Pattern shape
    - Bounds of the fitting
- **Paving**
  - Column vectors
    - Basis of the placement of the tiles
  - Repetition space
    - Bounds of the paving
  - Origin
    - Coordinates of the reference point of the reference tile

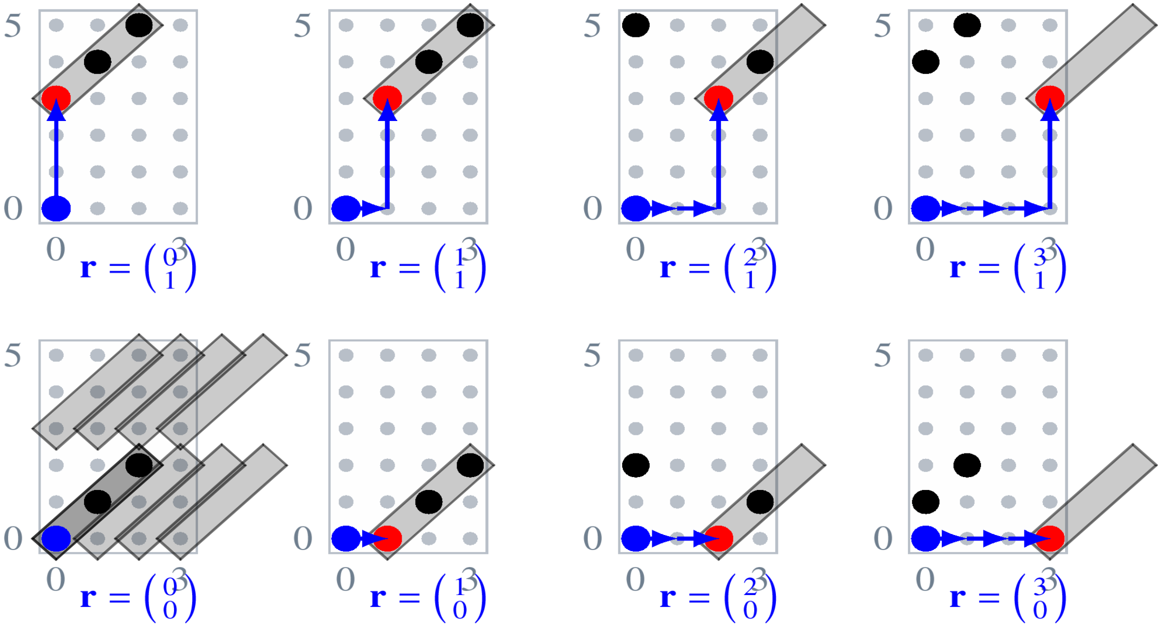
Graphical Interpretation of a Tiler (2/2)

$$F = \begin{pmatrix} 1 \\ 1 \end{pmatrix} \qquad \mathbf{s}_{\text{pattern}} = \begin{pmatrix} 3 \end{pmatrix}$$

$$\mathbf{o} = \begin{pmatrix} 0 \\ 0 \end{pmatrix} \qquad \mathbf{s}_{\text{array}} = \begin{pmatrix} 4 \\ 6 \end{pmatrix}$$

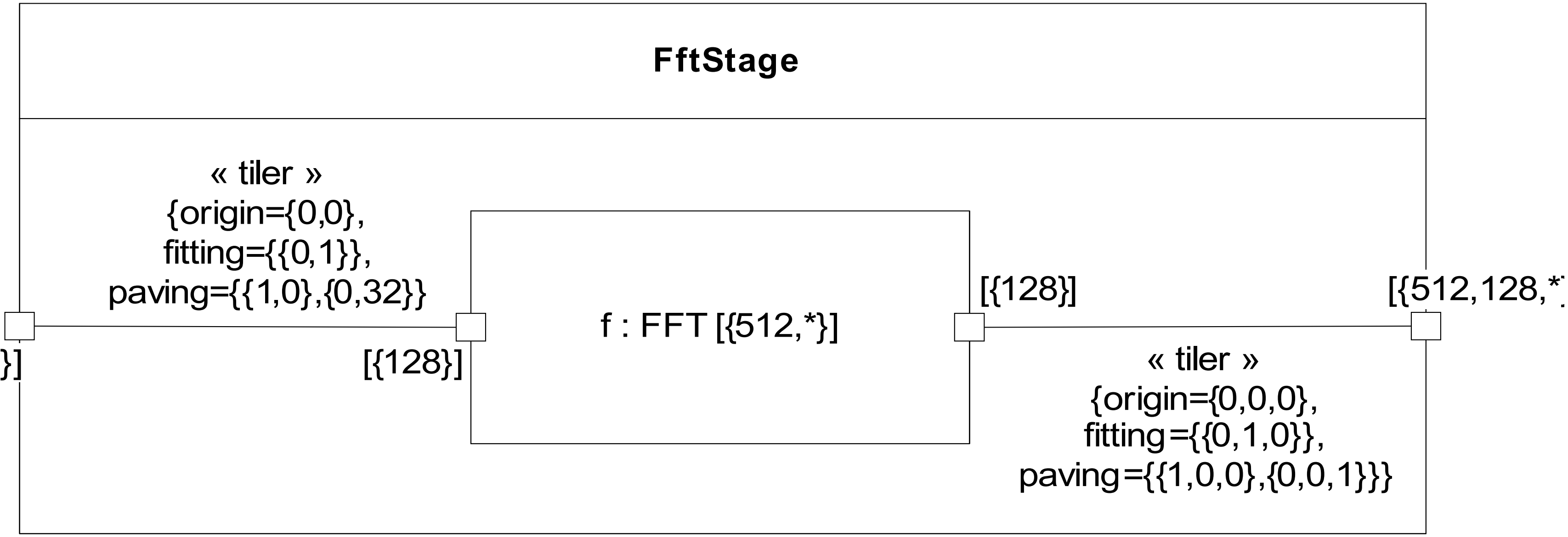
$$P = \begin{pmatrix} 1 & 0 \\ 0 & 3 \end{pmatrix} \qquad \mathbf{s}_{\text{repetition}} = \begin{pmatrix} 4 \\ 2 \end{pmatrix}$$




5
0
0
3
$\mathbf{r} = \begin{pmatrix} 0 \\ 1 \end{pmatrix}$
$\mathbf{r} = \begin{pmatrix} 1 \\ 1 \end{pmatrix}$
$\mathbf{r} = \begin{pmatrix} 2 \\ 1 \end{pmatrix}$
$\mathbf{r} = \begin{pmatrix} 3 \\ 1 \end{pmatrix}$
$\mathbf{r} = \begin{pmatrix} 0 \\ 0 \end{pmatrix}$
$\mathbf{r} = \begin{pmatrix} 1 \\ 0 \end{pmatrix}$
$\mathbf{r} = \begin{pmatrix} 2 \\ 0 \end{pmatrix}$
$\mathbf{r} = \begin{pmatrix} 3 \\ 0 \end{pmatrix}$

- **Fitting**
  - Column vectors
    - Basis of the tile
  - Pattern shape
    - Bounds of the fitting
- **Paving**
  - Column vectors
    - Basis of the placement of the tiles
  - Repetition space
    - Bounds of the paving
  - Origin
    - Coordinates of the reference point of the reference tile

Application Example



FftStage

« tiler »
{origin={0,0},
fitting={{0,1}},
paving={{1,0},{0,32}}

[{512,*}]

[{128}]

f : FFT [{512,*}]

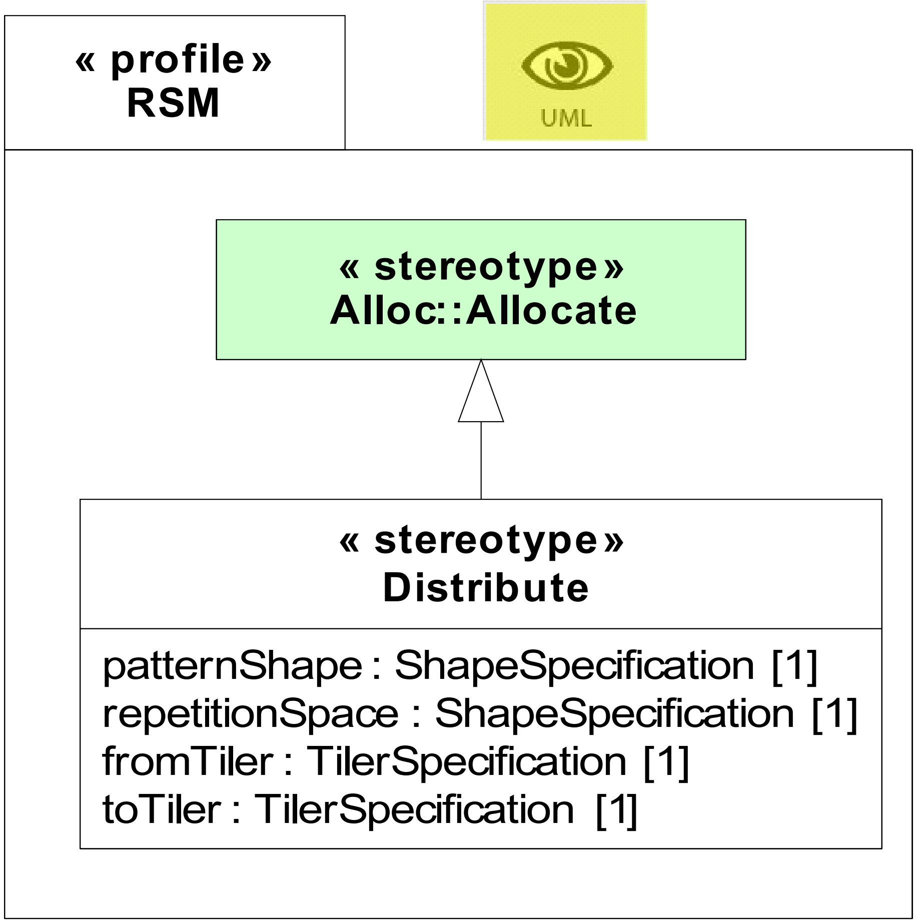
[{128}]

[{512,128,*

« tiler »
{origin={0,0,0},
fitting={{0,1,0}},
paving={{1,0,0},{0,0,1}}}

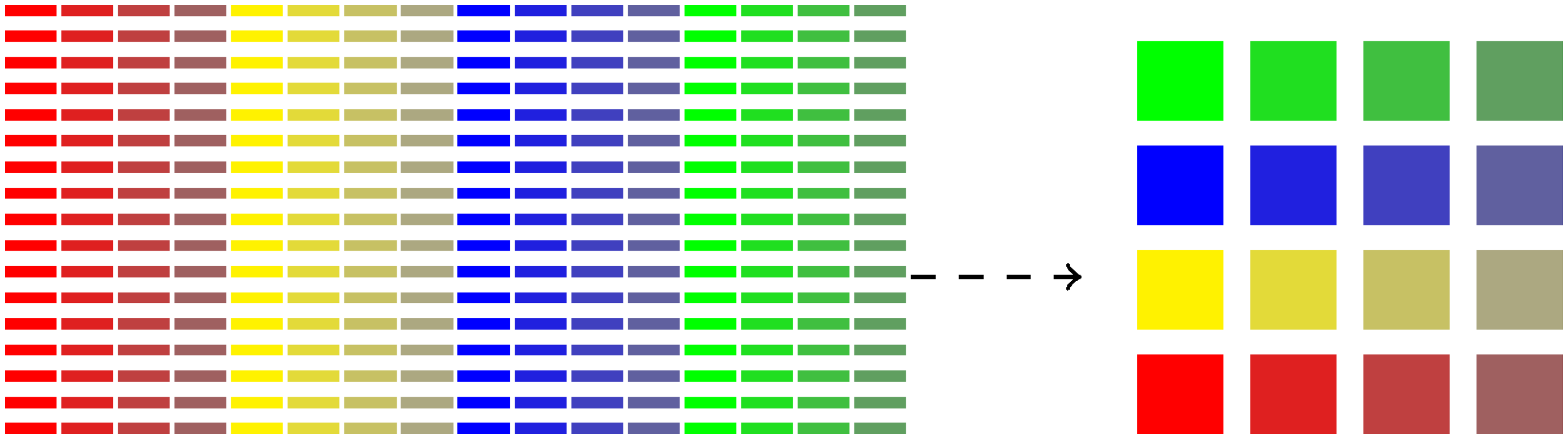
- **Samples from 512 hydrophones around a submarine**
  - Shape of the input data = 512×∞
- **Repetition of FFTs**
  - For each hydrophone
  - Sliding window of 128 samples every 32 time steps

Distribution


« profile »
RSM
UML
« stereotype »
Alloc::Allocate
« stereotype »
Distribute
patternShape : ShapeSpecification [1]
repetitionSpace : ShapeSpecification [1]
fromTiler : TilerSpecification [1]
toTiler : TilerSpecification [1]

- **Refinement of Allocation**
- **Similar to the reshape stereotype of the connectors**
- **Principle**
  - Tiling both ends
    - Two tilers
  - With the same tiles
    - One pattern shape
    - One repetition space
- **Power of expression**
  - At least all HPF data distributions

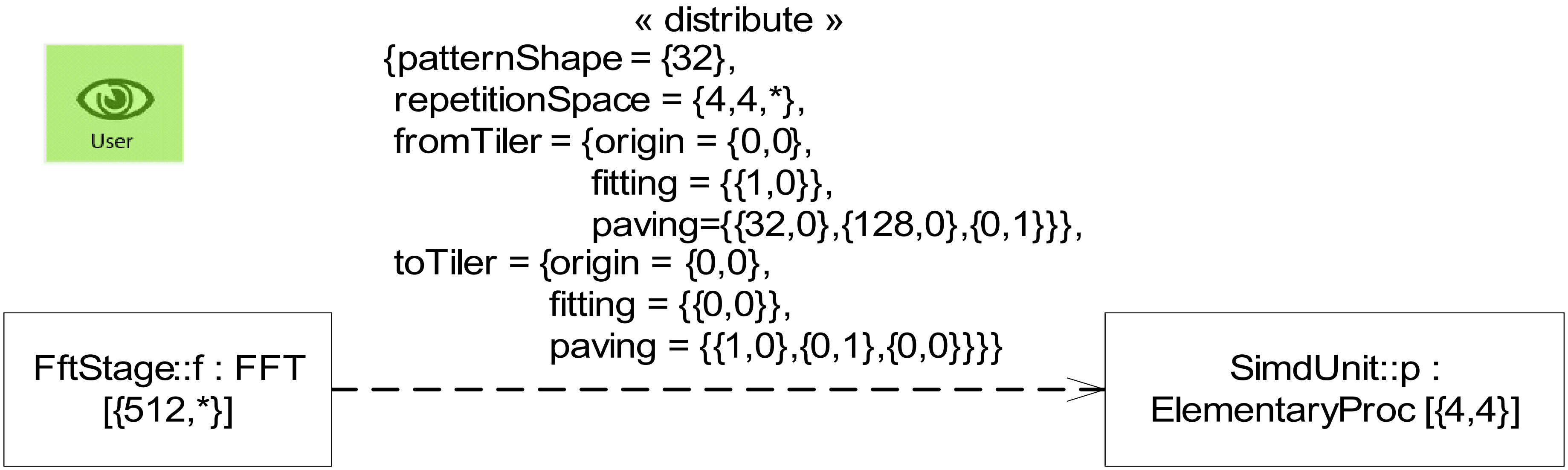
Distribution Example



- **Distribution of the FFT computations to the SIMD unit**
  - No spatial distribution of the infinite dimension (time steps)
  - Bloc distribution of the 512 FFTs for each time step
    - Size of the bloc = 32
    - On the 16 elementary processors

Distribution Example

User



```
« distribute »
{patternShape = {32},
 repetitionSpace = {4,4,*},
 fromTiler = {origin = {0,0},
                  fitting = {{1,0}},
                  paving={{32,0},{128,0},{0,1}}},
 toTiler = {origin = {0,0},
              fitting = {{0,0}},
              paving = {{1,0},{0,1},{0,0}}}}
```

FftStage::f : FFT [{512,*}]

SimdUnit::p : ElementaryProc [{4,4}]

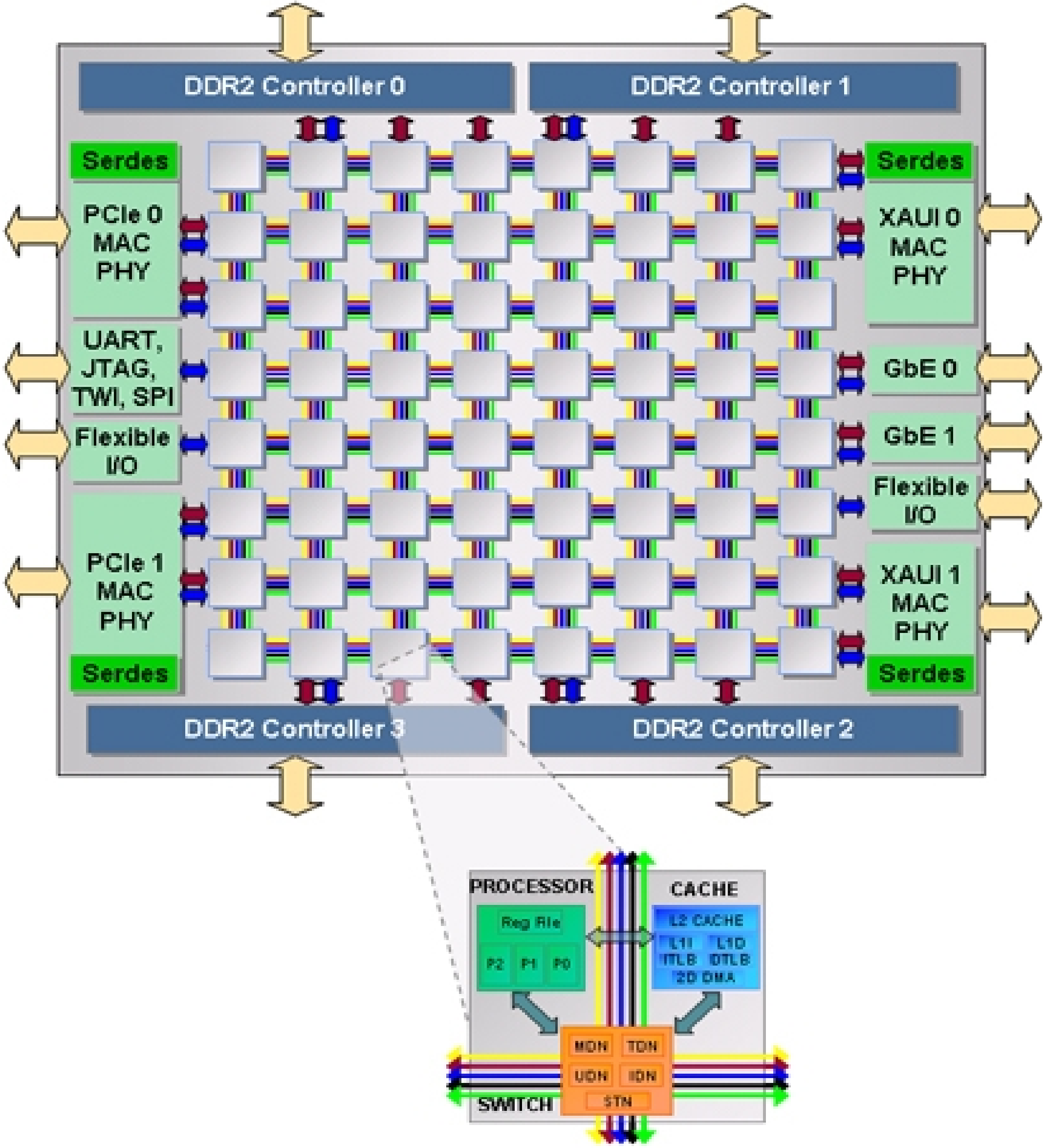
Distribution of the FFT computations to the SIMD unit

- No spatial distribution of the infinite dimension (time steps)
- Bloc distribution of the 512 FFTs for each time step
  - Size of the bloc = 32
  - On the 16 elementary processors

Complex Hardware Example:Tile64

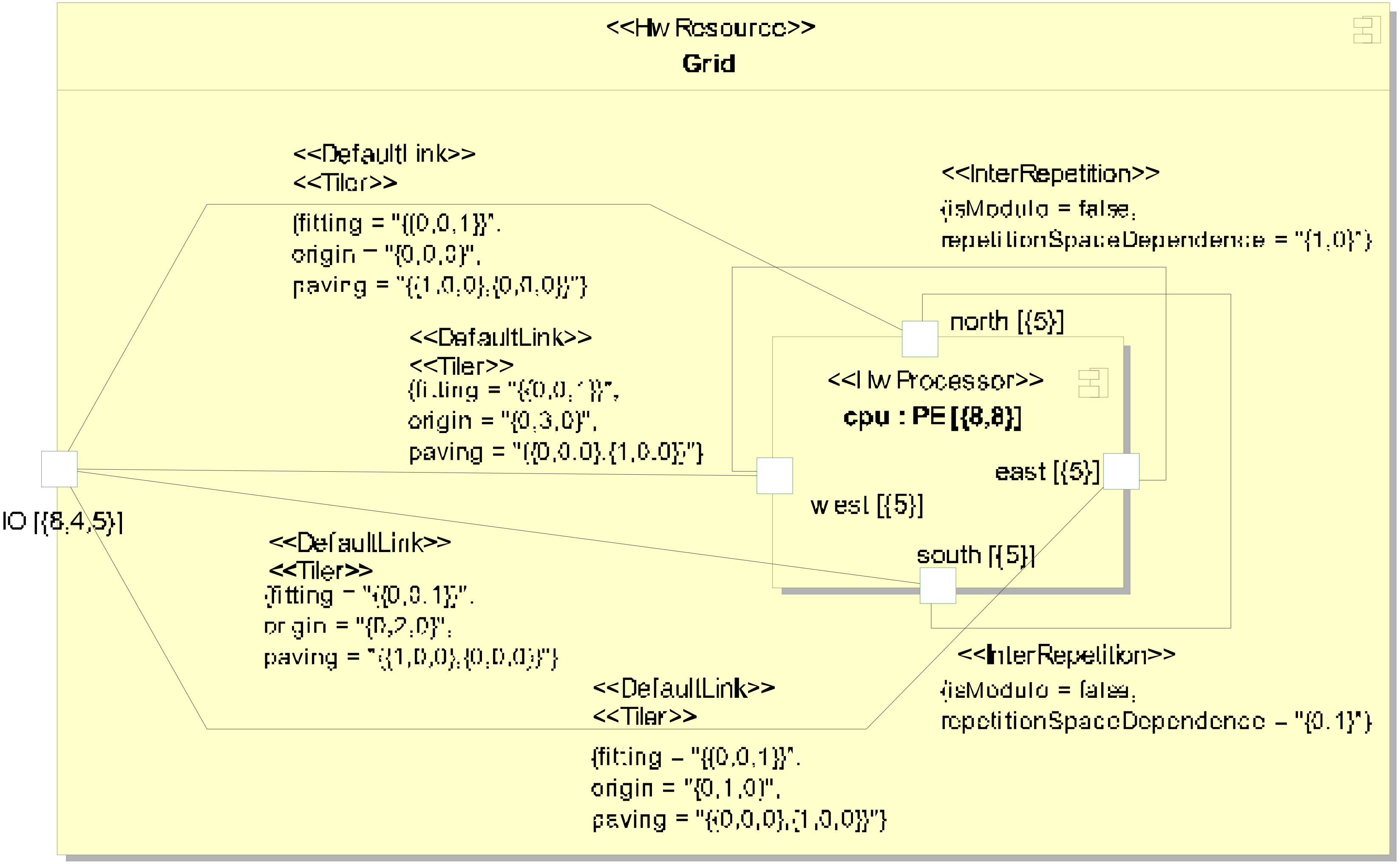
- **Challenge**
  - Model the architecture
  - In the most compact way

- **Proposal**
  - 8x8-repetition of the processing element
  - 4-repetition of the DDR2 controller
  - Factorization of the ports



Processing Element Repetition

User



<<HwResource>>
Grid

<<DefaultLink>>
<<Tiler>>
{fitting = "{{0,0,1}}",
origin = "{0,0,0}",
paving = "{{1,0,0},{0,1,0}}"}

<<InterRepetition>>
{isModulo = false,
repetitionSpaceDependence = "{1,0}"}

north [{5}]

<<DefaultLink>>
<<Tiler>>
{fitting = "{{0,0,1}}",
origin = "{0,3,0}",
paving = "{{0,0,0},{1,0,0}}"}

<<HwProcessor>>
cpu : PE [{8,8}]

east [{5}]

west [{5}]

IO [{8,4,5}]

south [{5}]

<<DefaultLink>>
<<Tiler>>
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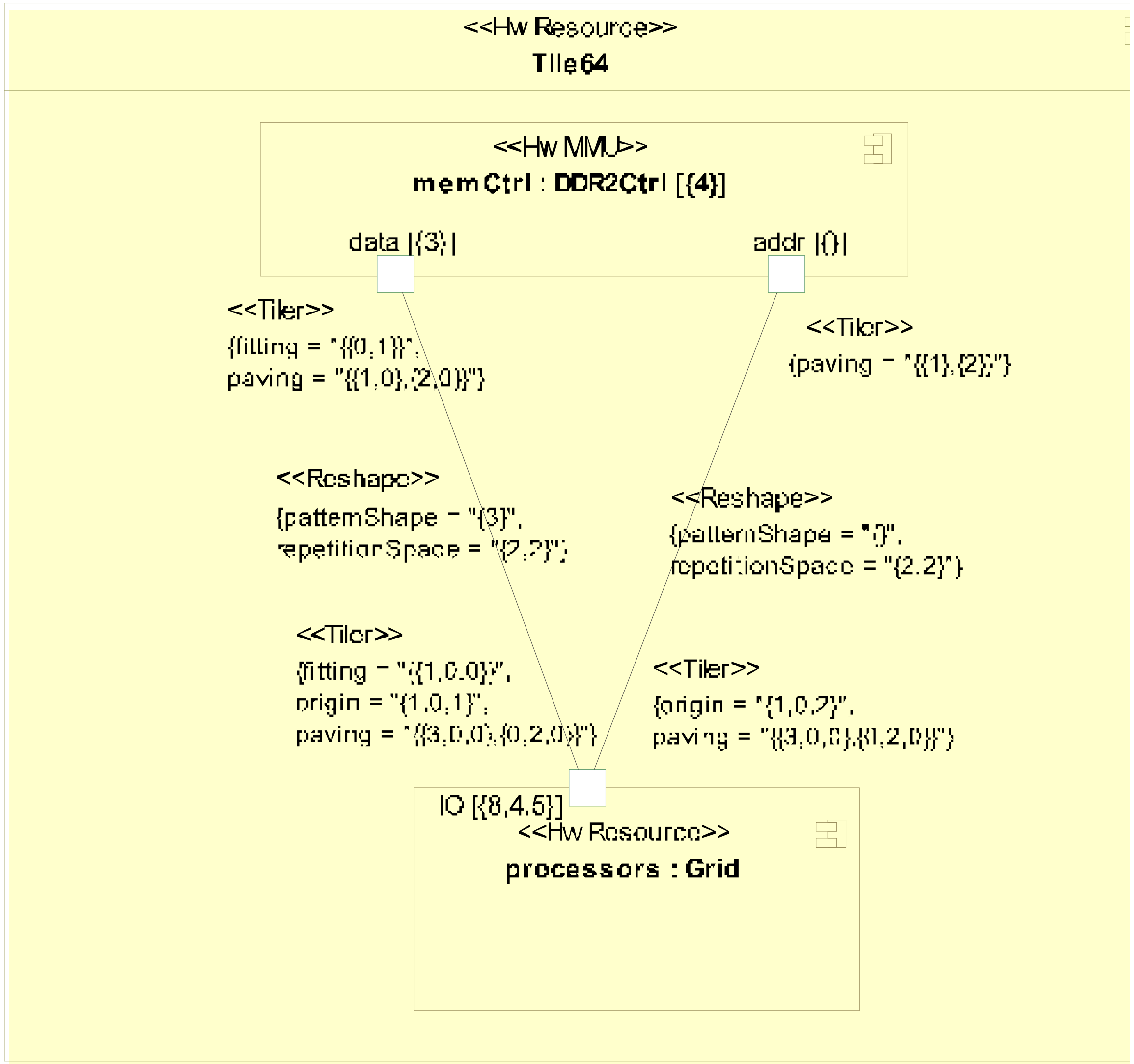
origin = "{0,2,0}",
paving = "{{1,0,0},{0,0,0}}"}

<<InterRepetition>>
{isModulo = false,
repetitionSpaceDependence = "{0,1}"}

<<DefaultLink>>
<<Tiler>>
{fitting = "{{0,0,1}}",
origin = "{0,1,0}",
paving = "{{0,0,0},{1,0,0}}"}

DDR2 Controler Connection to the Grid

User



Conclusion on RSM

- **General mechanism to handle**
  - Multidimensional structures (arrays)
  - Tiling by sub-structures (non orthogonal or sparse tiles possible)
  - Links between such structures (cyclic or non cyclic connection patterns possible)
- **Necessary to handle massive regular parallelism**
  - Compactness of the model
  - Efficiency, maintainability, readability
- **Relations with the rest of MARTE**
  - Uses VSL
  - Benefits from the component model (flow ports)
  - Applies to both application and hardware components
  - Extends allocation
- **Limitations**
  - Handles only arrays (no fancier shapes)
  - Would benefit from a custom (visual) tiler editor
    - Under development